Non-Volatile Ferroelectric Memory with Position-Addressable Polymer Semiconducting Nanowire

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One-dimensional nanowires (NWs) have been extensively examined for numerous potential nano-electronic device applications such as transistors, sensors, memories, and photodetectors. The ferroelectric-gate field effect transistors (Fe-FETs) with semiconducting NWs in particular in combination with ferroelectric polymers as gate insulating layers have attracted great attention because of their potential in high density memory integration. However, most of the devices still suffer from low yield of devices mainly due to the ill-control of the location of NWs on a substrate. NWs randomly deposited on a substrate from solution-dispersed droplet made it extremely difficult to fabricate arrays of NW Fe-FETs. Moreover, rigid inorganic NWs were rarely applicable for flexible non-volatile memories. Here, we present the NW Fe-FETs with position-addressable polymer semiconducting NWs. Polymer NWs precisely controlled in both location and number between source and drain electrode were achieved by direct electrohydrodynamic NW printing. The polymer NW Fe-FETs with a ferroelectric poly(vinylidene fluoride-co-trifluoroethylene) exhibited non-volatile ON/OFF current margin at zero gate voltage of approximately 10^2 with time-dependent data retention and read/write endurance of more than 10^4 seconds and 10^2 cycles, respectively. Furthermore, our device showed characteristic bistable current hysteresis curves when being deformed with various bending radii and multiple bending cycles over 1000 times.

1. Introduction

Ferroelectric-gate field effect transistors (Fe-FETs) using the spontaneous polarization of ferroelectric layers as gate insulators have a great potential in use of many current mobile applications such as cellphones, digital cameras, MP3 players, and USB memory sticks because of their various advantages including non-destructive readout,[1–3] low power consumption,[4–6] good retention, endurance,[7–9] fast response time,[10,11] multilevel operation[12–16] and scalable feature size of $4F^2$.[17] In particular, Fe-FETs with polymeric ferroelectric insulators are further beneficial due to their easy fabrication based on solution processes and mechanical flexibility, offering newly emerging products readily adaptable for non-planar geometries as well as repetitive dynamic mechanical motion such as bending, stretching and folding. It is also important appropriately to design semiconducting channels for realizing of flexible Fe-FETs. The semiconductors should be suitable for the mechanical deformation with firm interfacial adhesion to ferroelectric polymer layer.

Another important aspect to be considered as a non-volatile memory is to ensure high cell density. Besides several

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DOI: 10.1002/smll.201303814

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alternative approaches for high density memories including multi-stacked memories[18] and multileveled one,[12–16] the simplest and most straightforward way is directly to scale down the dimensions of an individual cell in particular channel size. These rather stringent conditions suggest that one of the most appropriate channel design is to fabricate nanowire (NW) channels based on polymer semiconductors. Furthermore, the polymer NWs should be easily addressable in desired locations for memory arrays.

Not to mention inorganic semiconductor NWs which have been extensively examined for numerous potential nano-electronic device applications such as transistors,[19–25] sensors,[26–28] memory,[29,30] and photodetectors,[31–33] great efforts have been also made to develop one-dimensional NWs of polymer semiconductors. The NW Fe-FETs have recently been fabricated with inorganic semiconductors such as Si[34] and ZnO[35] in combination with ferroelectric poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE) as gate insulating layers. The devices exhibited excellent memory performance arising from bistable charge carrier modulation in the NW channels controlled by the characteristic polarization switching of PVDF-TrFE. However, the previous work exhibited low device yield mainly due to the ill-control of the location of NWs on a substrate. NWs were vertically grown by chemical vapor deposition,[36] followed by the transfer of the NWs on a target substrate by depositing a dispersed NWs in solvent. The processes gave rise to NWs randomly placed on the substrate, making it difficult to develop arrays of NW Fe-FETs.[34,35] Moreover, rigid inorganic NWs have difficulties for applications to flexible non-volatile memories. Alternatively, inorganic NWs were developed by photolithography, followed by time-consuming multiple dry etching steps.[30]

Direct electrohydrodynamic NW printing is, previously reported, a novel technique which can fabricate and align the organic NWs with desired position and orientation using electrostatic force and high speed linear motor stage.[37] It employs the strong electric field between a nozzle tip and a grounded collector. When a viscous polymer solution is ejected from the nozzle tip, it is stretched by the electrostatic force and deposited onto the grounded collector. Because the tip-to-collector distance is very short as much as a few millimeters, perturbation or bending instability of jetted solution is suppressed, which results in straight ejection of polymer jet. As moving collector connected to the high speed linear motor stage, we can align the NWs with desired position and orientation. Using direct electrohydrodynamic NW printing, we demonstrated the highly aligned organic semiconducting NWs and their application to transistor in the previous study.[37]

In this paper, we demonstrate a novel polymer NW Fe-FET with a position-addressable semiconducting polymer NW channel and ferroelectric polymer insulator. The direct electrohydrodynamic NW printing was employed to develop large-scale assembly of highly aligned semiconducting poly(3-hexylthiophene) (P3HT) NWs, allowing for precise control of location as well as number of NWs between source and drain electrode. Memory performance was systematically investigated as a function of the number of NWs in the channel regions. Our polymer NW Fe-FETs with carefully controlled NW/PVDF-TrFE interface exhibited large ON/OFF current margin of approximately 10^2 with time-dependent data retention and read/write endurance of more than 10^4 seconds and 10^2 cycles, respectively. Furthermore, they are mechanically flexible, and thus suitable for multiple bending circumstance.

2. Results and Discussion

A polymer NW Fe-FET memory device with a top-gate bottom-contact (TGBC) structure consisting of an Au source-drain (S/D) electrode/polymer NW/PVDF-TrFE/Al gate electrode was constructed on either a Si/SiO_2 wafer or a flexible polymer substrate as schematically illustrated in **Figure 1**a. A well-aligned polymer NW of approximately 300 nm in diameter consisting of semiconducting core and insulating thin shell was directly deposited onto the patterned Au S/D electrodes by electrohydrodynamic NW printing from a P3HT (semiconductor)/poly(ethylene oxide) (PEO) (insulator) blended solution (70:30, w/w), giving rise to well defined channel across S and D electrode.[37] Subsequently, the polymer NWs were annealed for 10 min at 180 °C to make PEO shell dewetted on P3HT surface for reliable memory performance as explained in details later. A 400 nm thick PVDF-TrFE layer (5 wt% in methyl ethyl ketone (MEK) solvent) was spin-coated onto the polymer NW, followed by thermal evaporation of the Al gate electrodes. To isolate between two cells as well as to make the Au S/D electrode accessible to contact probes, the PVDF-TrFE layers in the regions outside the areas covered by the top Al electrodes were etched by O_2 plasma using reactive ion etching (RIE), finalizing the fabrication of a polymer NW Fe-FET device as also schematically shown in Figure 1a. The PVDF-TrFE layer embedded with 300 nm polymer NW was visualized using scanning electron microscopy (SEM), as shown in Figure 1b. Considering that the previous non-volatile memories with semiconducting NW channels have difficulty in positioning the NWs at the desired position and thus arrays of the devices have been rarely demonstrated,[29,34,35] our approach using electrohydrodynamic NW printing process is extremely advantageous. In fact, we fabricated highly aligned nonvolatile memory arrays with the number of NWs precisely controlled from 1 to 16 as shown in the optical microscope (OM) images of Figure 1a. The spacing between NWs was controlled by the motorized linear stage, and the uniformity of spacing was determined by the resolution of equipment. However, because the accuracy of alignment is greatly influenced by perturbation sources such as the vibration of equipment or air flow, the resultant aligned NWs were likely to have spacing between two wires with a little variation. In addition, as the spacing of wires decreased, repulsive force from residual charges on the surface of NWs might act to decrease the degree of alignment during printing. In this work, we aligned the P3HT/PEO NWs on the Si/SiO_2 substrate. Because residual charges on the surface of printed NWs were not discharged rapidly due to the insulating SiO_2 substrate, repulsion between the wires would grow bigger.

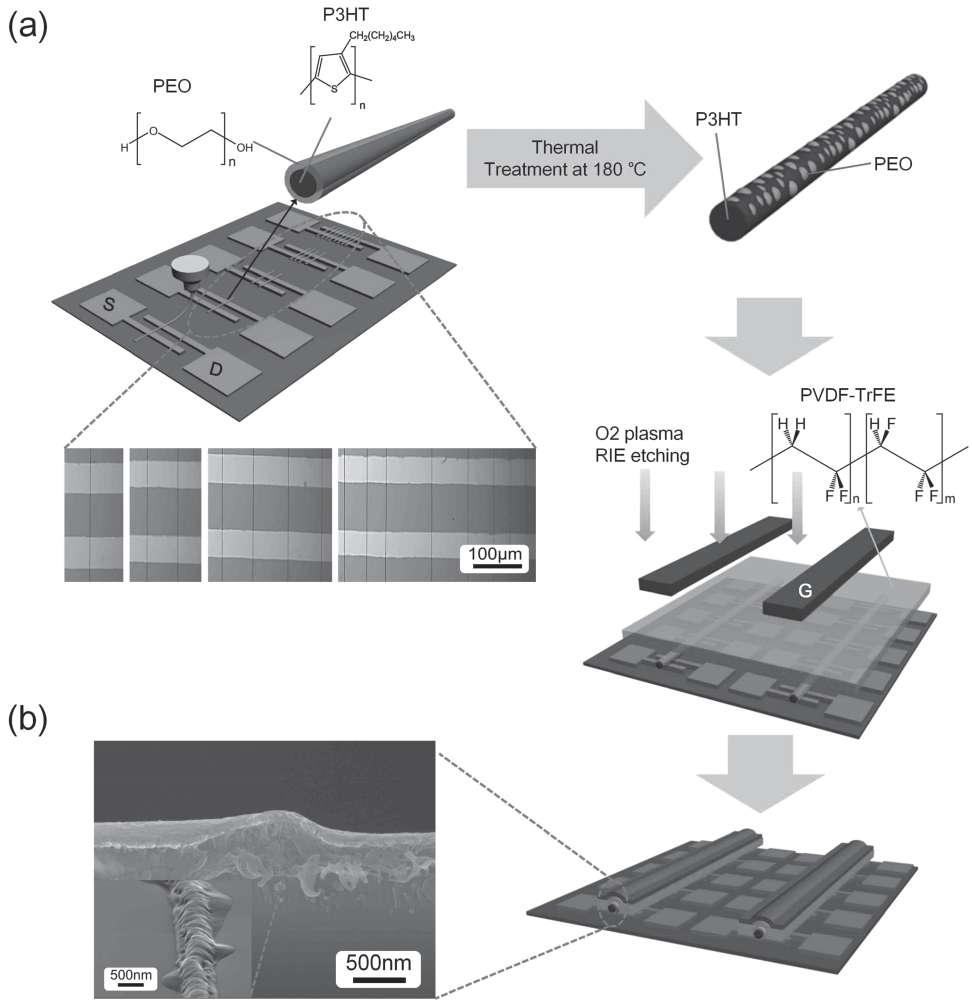

Figure 1. (a) A schematic illustration of the fabrication process for the top-gate bottom contact Fe-FET memory device with a P3HT:PEO-blend (70:30, w/w) NW channel and ferroelectric insulator. Optical micrograph images of highly aligned polymer NW Fe-FET memory arrays with precisely controlled NW numbers (bottom). Thin PEO shell was dewetted on P3HT NW after thermal treatment. (b) A SEM image showing the cross-sectional of the PVDF-TrFE layer embedded with 300 nm polymer NW of the Fe-FET. The inset shows a SEM image of the thermal treated P3HT NW on the SiO_2 substrate.

The polymer NW Fe-FET with the P3HT wire channel exhibited p-type output characteristics in the source-drain current (I_{DS}) versus source-drain voltage (V_{DS}) curve and the transfer curve (at a V_{DS} of –20 V) with hysteresis loop as a function of a gate voltage (V_G), as shown in **Figure 2**a and 2b, respectively. The I_{DS} hysteresis in the transfer plot arose from the voltage-dependent ferroelectric polarization switching of a PVDF-TrFE gate insulator as extensively studied in the previous works.[1,2,6,16] After the device was turned on, there was a rapid increase of the I_{DS} with a negative bias in V_G owing to accumulation of excess holes in the P3HT NW channel. When the V_G returned to zero, the I_{DS} still stayed saturated due to the remanent polarization of PVDF-TrFE layer with non-volatile H-F dipoles in which fluorine atoms pointed to the P3HT NW. The following application of a positive V_G sufficiently larger than coercive field of the PVDF-TrFE layer on the device progressively switched the H-F dipoles, leading to a decrease in the I_{DS} (as shown the inset of Figure 2b). Upon removal of the positive V_G, the depleted state of P3HT channel with the low I_{DS} remained, which allowed for memory operation with distinct bistable ON (high) and OFF (low) current states.

The ON current level was readily controlled in our device simply by changing the number of NWs between S and D electrodes. We systematically investigated the *I–V* characteristics of the devices, depending on the number of polymer wires; the results are shown in Figure 2c and 2d. Apparently, ON current increased with the number of NWs due to the increase of channel area as shown in Figure 2c and Supporting information, Figure S1. Because of the variation of OFF current level of the devices which was also affected by gate leakage current between G and D electrodes, rather large fluctuation of ON/OFF current ratio was observed as shown in Figure 2d. In particular, ON/OFF ratio of a device with 16 wires was varied more than those of other devices with different number of wires but the average ratio of the device was still greater than 10^2, which was sufficient for non-volatile memory operation. (also see Supporting information, Figure S2) As shown Figure S2 in which the ON and OFF currents of NW Fe-FETs at V_G 0 V, V_{DS} –20 V were plotted

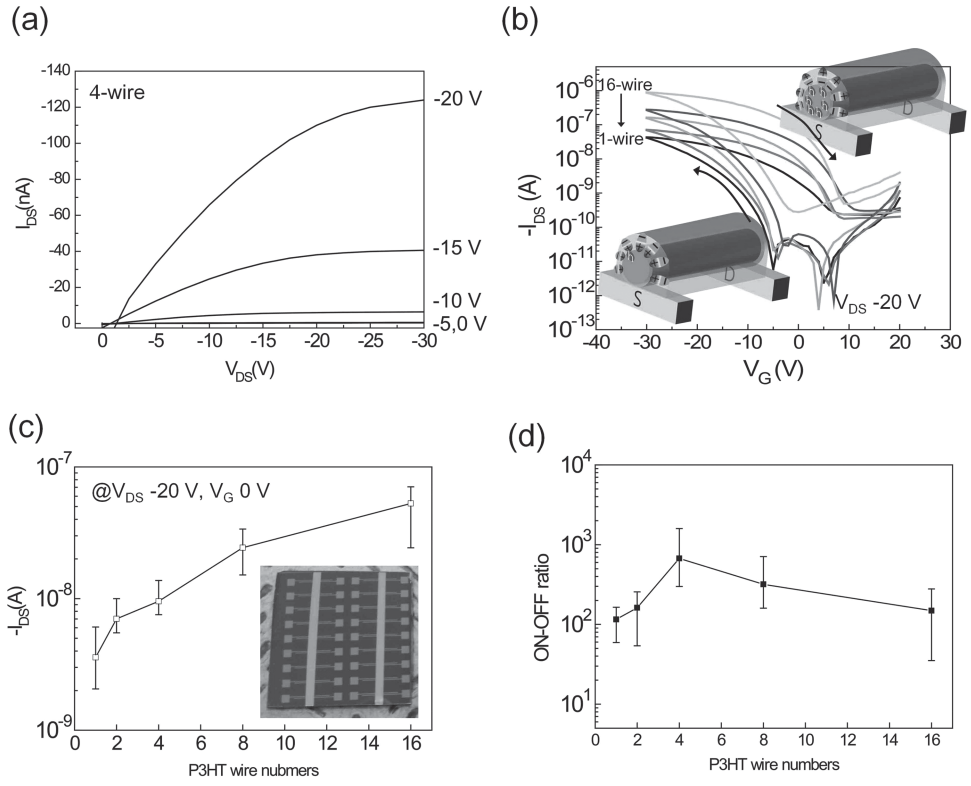

Figure 2. (a) Representative *I–V* output plots and of a polymer NW Fe-FET device with 4 wire channel. (b) I_{DS}–V_G transfer curves of the device demonstrating characteristic current hysteresis arising from the non-volatile ferroelectric polarization of the PVDF-TrFE layer. (c) The ON current and (d) ON/OFF ratios of the devices with the different number of polymer wires. The inset of (c) shows a photograph of the arrays of devices. The distribution of both ON current values and ON/OFF ratios was calculated by the standard error of sets of more than 5 cells.

as a function of the numbers of NWs, rather large fluctuation of OFF current was observed with a Fe-FET with 16 wires. We believe that the fluctuation arose from the variation of PEO shell in thickness. Since the PEO shells were developed by phase segregation with P3HT during electrohydrodynamic NW printing process, their thickness was hardly controlled in particular after thermal treatment for the dewetting of PEO. When the number of NWs increased, the statistical variation of PEO shell thickness became larger, resulting in the large cell-to-cell variation of OFF current. ON/OFF ratio values of the devices slightly increased with the number of wires and remained approximately 700 on average when the devices contained 4 wires and more as shown in Figure 2d. (Supporting information, Figure S2). Our results indicate that memory property can be controlled by adjusting the number of wires with the precise control of their location.

Reliable operation of our polymer NW Fe-FET memory is also of prime importance including time dependent data retention and write/erase cycle endurance. First of all, we investigated the data retention of a device over time; the results are shown in Figure **3**a. Data retention was evaluated by independently measuring bi-stable non-volatile I_{DS} values set by different gate voltage sweeps at $V_G = -10$ V with a constant V_{DS} of –20 V. Figure 3a shows reliable data retention of two distinct states for up to approximately 10^4 seconds. The time-dependent data retention results of more than 10^4 seconds of our devices are very comparable with those of previous works.[34,35] For multiple data write/erase endurance measurements, we consecutively read two-level non-volatile I_{DS} values with the programmed endurance cycle. The sequence used was erase/read/ program/read with two corresponding DC program gate sweeps of +20–0 V and –30–0 V. Very consistent and reliable rewritable two-level cycles were observed over 120 cycles, as shown in Figure 3b. Our polymer NW Fe-FET memory is beneficial because of the nondestructive device operation with a FET architecture based on polarization switching, which is electrically much more stable than conduction switching.[38–43]

Operation time characteristics of our polymer NW Fe-FET are also important. Although intrinsic switching of a PVDF-TrFE exhibited in approximately a few nano second level, its switching speed was varied, following the kinds of devices.[44] As an example, metal/ferroelectric/metal capacitors exhibited in general switching time of an order of micro seconds while field effect transistor type devices showed switching time of 10^{-3} to 10^{-4} seconds.[45–47] These are not directly correlated with organic semiconductor field effect mobilities ranging from 0.05 to approximately 1 cm^2/Vs either. Since our NW Fe-FET with P3HT channel having the field effect mobility of approximately 0.01 cm^2/Vs would certainly show the switching behavior similar to those from previous works. At first sight, it might seem unfortunate that Fe-FET with a ferroelectric polymer cannot be suitable for high speed memory applications. The literature, however, suggests that our FET device can be used for applications requiring kHz level frequency operation.

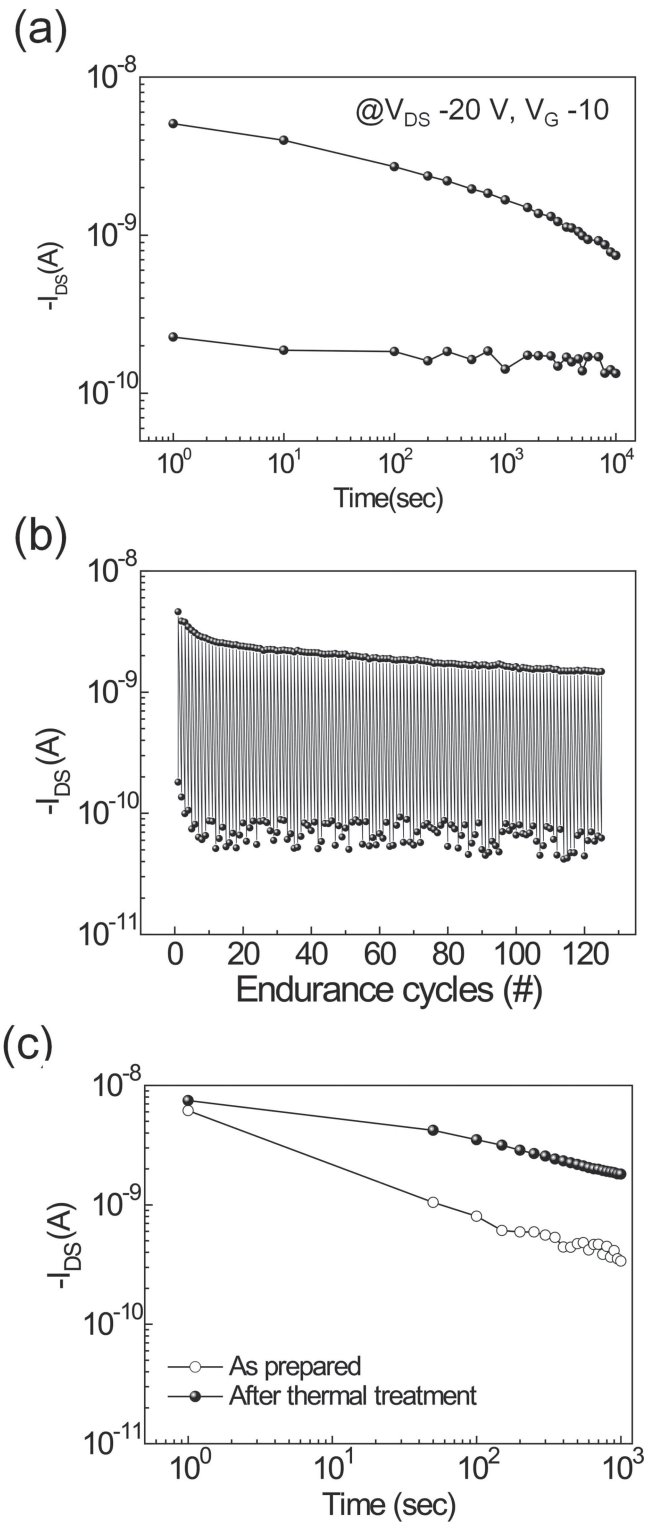

Figure 3. (a) The time-dependent retention characteristics and (b) write/erase endurance cycles of I_{DS} values established in a polymer NW Fe-FET. (c) The retention data of the ON current of a NW Fe-FET before and after thermal treatment of the polymer NW.

Unfortunately, most of the devices with NWs without thermal treatment did not exhibit reliable data retention properties. For instance, as shown Figure 3c, a Fe-FET with 4 as-prepared and non-thermal treated polymer NWs suffered from poor ON current data retention with significant drop of an initial current level within 1000 seconds, giving rise to ON/OFF memory margin of approximately 10 possibly due to extra hole carriers trapped by the ether groups of PEO shell. Oxygen atoms in ethers readily form the hydrogen bonds with water molecules, one of the origins of threshold voltage instability of a thin film transistor. Water molecules diffused into the PEO layer are known to generate deep hole traps, leading to threshold voltage shifts as we observed in Figure S3.[48,49]

To further reveal the origin of the ON current decrease of our device with time, we fabricated three model devices with planar semiconducting channels: Fe-FETs with (1) a P3HT film, (2) a solution-blended PEO/P3HT (30/70) film and (3) bilayered PEO/P3HT film. (see Supporting information, Figure S4) The Fe-FET with only P3HT channel exhibited a reliable non-volatile memory performance with stable date retention over 10^3 sec while ON current levels of the devices with both blended and layered PEO progressively decreased with time and reached at a current level close to the OFF current one. (Supporting information, Figure S4) The results clearly suggest that the poor retention characteristics of our polymer NW Fe-FET arose from the presence of PEO in the channel. It should be also noted from Supporting information, Figure S4 that the ON current levels of the devices containing PEO at negative bias are lower than that of the device without PEO because hole carrier accumulation in P3HT channels of PEO containing Fe-FETs was suppressed by the trapped holes in the PEO regions, which again supports our claim of the role of PEO. Another evidence of the trapped holes in the PEO is the threshold voltage shift to negative gate bias in a device with bilayered PEO/P3HT film. Higher negative bias was required to compensate the trapped holes and in turn to turn on the device.

Figure 4a shows a proposed mechanism of the degraded data retention of our polymer NW Fe-FET. Extra holes were trapped into PEO (shell) at initial state as shown in the left scheme. When a V_G above –30 V was applied, the fluorine atoms of PVDF-TrFE layer point to the P3HT/PEO NW due to spontaneous polarization built up in the ferroelectric layer, leading to accumulation of excess holes in the P3HT layer. During retention test at a relatively low read voltage, the extra holes trapped in the PEO were easily de-trapped and moved into defect sites at the PEO/PVDF-TrFE interface with time,[50] followed by the interaction with the aligned H-F dipoles in PVDF-TrFE as shown in the middle scheme of Figure 4a. The depolarization of H-F dipoles due to the migrated excess holes at PEO/PVDF-TrFE interface in turn mitigated the accumulation of excess holes in P3HT channel, leading to decrease of channel current over time as shown in the right scheme of Figure 4a. The consequent gradual depletion of P3HT NW channel with time resulted in the poor retention characteristics of our device.

It is, therefore, apparent that the retention properties of our device were improved when a direct interface between PVDF-TrFE and P3HT was formed by dewetting PEO interlayer. During the thermal treatment 10 min at 180 °C well above melting temperature of PEO (T_m = 65 °C), PEO molecules with sufficiently low viscosity at such a high

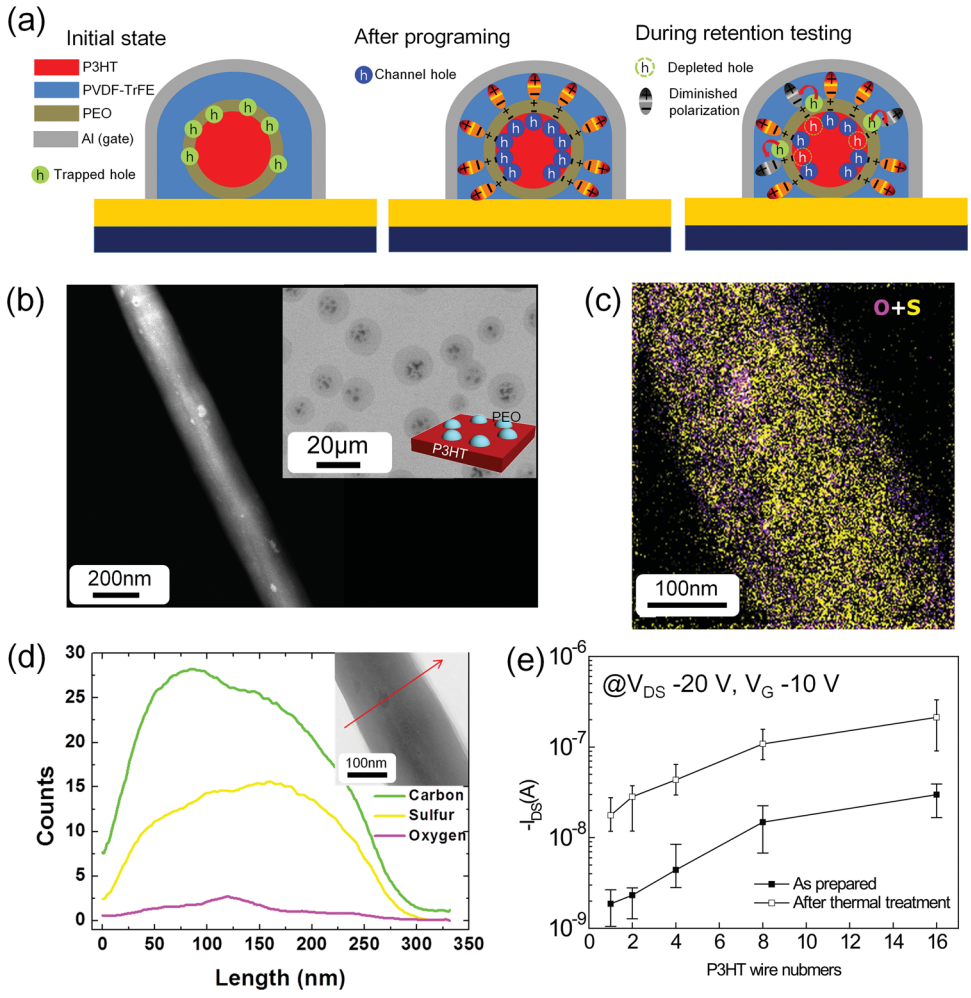

Figure 4. (a) Schematic diagrams illustrating the degradation mechanism of the data retention of a polymer NW Fe-FET due to PEO interlayer. (b) A TEM image of a polymer NW and a SEM image (inset) of the bilayered PEO/P3HT film after thermal treatment, respectively. The scheme in the inset exhibits PEO domains dewetted on P3HT upon thermal treatment. (c) EELS mapping of oxygen (purple)/sulfur (yellow) atoms of the thermally treated NW (left) clearly shows spacially isolated oxygen aggregates, indivative of the dewetting of PEO on P3HT NW. (d) EDS line mapping of carbon, sulfur, and oxygen atoms along red arrow across the NW in the inset of TEM image indicates the exposure of P3HT on the NW surface. (e) The ON current values of the devices as a function of the number of polymer wires before and after thermal treatment.

temperature were dewetted on P3HT core whose shape had been rarely altered at 180 °C due to its high melting temperature of approximately 238 °C. It should be noted that PEO should be included in our NW printing in order to adjust the solution viscosity for successful jetting of the solution without breakage. The morphological and compositional information of the polymer NW after thermal treatment was obtained by transmission electron microscopy (TEM), electron energy-loss spectroscopy (EELS) and energy dispersive X-ray spectroscopy (EDS) elemental analysis, as shown Figure 4b, 4c and 4d. Upon heating process, the PEO shell of a NW was molten and spread on P3HT core, rendering the width of the NW become larger. EDS results of bilayerd PEO/P3HT film also showed the exposure of P3HT surface in air due to the dewetting of PEO. (Supporting information, Figure S5b) EELS and EDS results of thermally treated P3HT/PEO NW again displayed that the signal from Oxygen K series was detected at dewetted PEO phase on P3HT surface. (Figure 4c and 4d) These results indicate the exposure of P3HT surface in air due to the dewetting of PEO. Furthermore, as shown Figure 4e, the higher ON current level as well as the lower threshold gate voltage of our device with thermally treated NWs were observed than the properties of a device with as-prepared NW, which again supports our argument of suppression of carrier accumulation in P3HT channel by the trapped holes in the PEO regions (Supporting information, S4).

More detailed dewetting behavior of PEO on P3HT surface was examined with a PEO-on-P3HT bilayer as shown in Supporting information, Figure S5. A very smooth PEO layer on P3HT film was certainly dewetted after very short thermal treatment at 180 °C for 5 seconds. Dewetting of PEO initiated with heterogeneous nucleation gave rise to randomly distributed macroscopic holes in PEO layer and the underlying P3HT was clearly exposed as shown Figure S5a. The macroscopic holes grew with time, followed by coalescence of the holes with each other in the time range of 5 to 25 seconds. The resulting polygons of PEO were broken at the final stage of the dewetting, giving rise to isolated droplets on P3HT with their diameter of approximately 20 to 30 μm as shown in Figure S5.

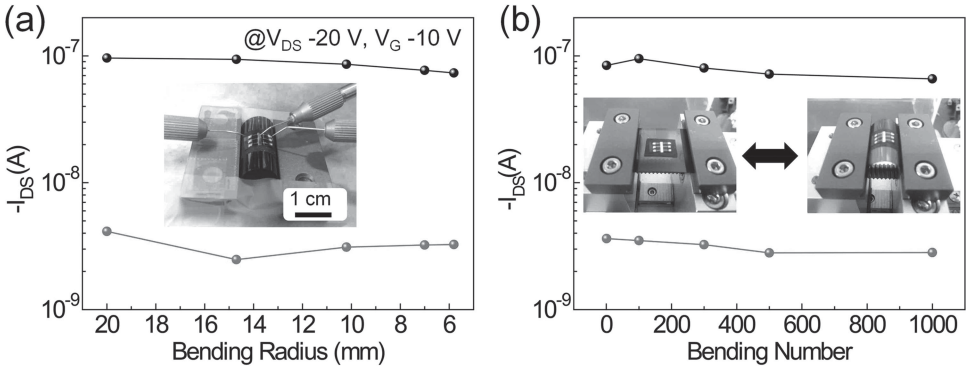

Figure 5. The ON and OFF current of a flexible polymer NW Fe-FET with 4 wire channel (a) as a function of the bending radius and (b) as a function of the number of bending cycles at a bending radius of 5.8 mm.

One of the main advantages using position-controlled polymer NW channels is that they are potentially suitable for arrays of mechanically flexible polymer NW memories. In fact, the arrays of polymer NW Fe-FETs fabricated on a commercially available polyimide substrate also showed reliable two state non-volatile *I–V* characteristics similar to those on SiO_2 (Supporting information, S6a). The device exhibited characteristic bi-stable current hysteresis curves upon the application of a gate voltage sweep when being deformed as a function of the bending radius (Supporting information, S6b and S6c). The ON and OFF current values at a read voltage of –10 V under in-situ bending conditions were similar, without any notable current fluctuation even in the low bending radius regime, as shown in **Figure 5**a. The flexible polymer NW memory was also robust with a consistent ON and OFF current margin after more than 1000 bending actions with a radius of 5.8 mm, as illustrated in Figure 5b.

3. Conclusion

We developed non-volatile polymer memories based on solution-processed polymer semiconducting NWs and ferroelectric PVDF-TrFE. Using our high throughput direct electrohydrodynamic NW printing, we efficiently fabricated large-scale assembly of aligned semiconducting P3HT NWs with excellent controllability of both location and number of NWs between source and drain electrodes. Memory performance arising from ferroelectric polarization switching of PVDF-TrFE was thus readily tuned with the number of NWs in the channel regions. In particular, the dewetting of PEO covered on P3HT NWs upon printing process using rapid thermal treatment significantly improved the reliability of a memory device by ensuring the direct interface between P3HT NW and PVDF-TrFE. The resulting device exhibited characteristic current hysteresis with data retention of longer than 10^4 seconds and write-erase endurance cycles of over 100 times, respectively. More importantly, a mechanically flexible polymer NW memory device was realized and tolerant upon the application of more than 1000 bending cycles at a bending radius of 5.8 mm. In summary, we report here a novel approach to offer a design strategy for low-cost high-density polymer memory and are conveniently adoptable for various flexible and foldable organic electronic devices.

4. Experimental Section

Materials and Film Preparation: PVDF-TrFE with 25 wt% TrFE was purchased from MSI Sensors. P3HT (Mw = 45 570 g mol^{-1} with 90% head to tail regioregularity) and PEO (Mw = 400 000 g mol^{-1}) purchased from Sigma Aldrich were used to prepare 70:30 (w/w) blend solutions of P3HT:PEO. Trichloroethylene (TCE) and chlorobenzene were mixed in appropriate ratio and used as the cosolvent of the P3HT:PEO-blend solution. The blended P3HT solution was injected into the metal nozzle with the inner diameter of 100 μm and P3HT:PEO-blend NWs were fabricated and aligned on a SiO_2 (500 nm) substrate with patterned Au S/D electrodes using the electrohydrodynamic NW printer. The fabricated polymer NWs were dried under vacuum for 2 h at 60 °C or annealed for 10 min at 180 °C. PVDF-TrFE solution in MEK with various blending ratios was spin-coated at 1500 rpm for 60 s on a polymer NW layer.

Polymer NW Fe-FET fabrication and characterization: SiO_2 substrates were cleaned in an ultrasonic bath with acetone and ethanol for 1 hour each. First, arrays of 30-nm-thick Au S/D electrodes with the width and length of 1000 and 100 μm, respectively were thermally evaporated on a substrate with a patterned shadow mask under a vacuum of 10^{-6} Torr. Subsequently, the polymer NW of approximately 300 nm in diameter was directly printed onto the patterned Au S/D electrodes by electrohydrodynamic NW printing. After thermal treatment at 60 °C or 180 °C, the ferroelectric insulator was spin-coated on a polymer NW layer. The PVDF-TrFE solution in MEK did not affect the underlying polymer NW layer. The insulator layer was annealed at 135 °C on a heating stage (Linkam 600, UK) for 2 h. The 70-nm-thick top gate Al electrodes were deposited by thermal evaporation under a vacuum of 10^{-6} Torr with a patterned shadow mask aligned with respect to the S/D electrodes previously formed. In order to make the Au S/D electrode accessible with contact probe tips, the devices were further treated with oxygen plasma (100 W for 200 s, 10^{-3} Torr, 40 sccm) generated by reactive ion etching (RIE) (Femto VITA-4E). Arrays of Al gate electrodes were used as RIE blocking masks, giving rise to top-gate-bottom-contact polymer NW Fe-FET memories with S/D electrodes open to the air, as illustrated in the schematic in Figure 1a. The electrical characteristics were measured using

a semiconductor system (E5270B, Agilent Technologies) under ambient conditions.

Structure Characterization: The morphological and compositional information of the polymer NW was characterized using field emission scanning electron microscopy (FESEM, JEOL-7001F) and transmission electron microscopy ((TEM, JEOL JEM-2200FS with Cs-corrector) (National Institute for Nanomaterials Technology, Korea) at an acceleration voltage of 200 kV without staining. An optical microscope (OM) was used to visualize the polymer NW Fe-FET devices (Olympus BX 51M).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This research was supported by the Converging Research Center Program through the Ministry of Science, ICT and Future Planning, Korea (2013K000183), the third Stage of Brain Korea 21 Plus Project in 2013 and Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (2010–0019313, 2012–0009460). This research was also supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2007–0056091).

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Received: December 13, 2013
Revised: January 29, 2014
Published online: March 18, 2014