

ORIGINAL ARTICLE

Charge transport and morphology of pentacene films confined in nano-patterned region

Tae-Sik Kim¹, Se Hyun Kim², Mi Jang³, Hoichang Yang³ and Tae-Woo Lee¹

The transport and morphology of macroscopic organic transistors have been thoroughly explained. However, the relationship between charge transport and the morphology of organic semiconductors in nano-confined regions is not well understood, which is required to design high-performance nano-electronics. Therefore, in this study, the electrical performance of pentacene thin-film transistors (TFTs) fabricated on nano-scale confined geometries was compared with that of other TFT systems fabricated on micro-scale confined or flat dielectrics. The results showed that the photoresist (PR) reliefs patterned onto silicon dioxide (SiO₂) dielectrics could control the growth mode of pentacene in the confined regions. As the line spacing between the PR patterns decreased to below the average size of pentacene normally grown on SiO₂ dielectrics ($\sim 1.7\ \mu\text{m}$), field-effect mobility (μ_{FET}) of pentacene TFTs improved considerably. Specifically, the μ_{FET} values for the 250 nm patterned dielectric system were as high as $0.33\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$, which was greater than those of the wider-patterned PR or flat dielectric systems ($\leq 0.15\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$). These findings were related to the enhancement of charge-carrier transport owing to the anisotropic π -conjugated crystals nucleated from the nano-confined edges, providing important information that can be used in the design of high-performance nano-scale organic electronics.

NPG Asia Materials (2014) 6, e91; doi:10.1038/am.2014.3; published online 14 March 2014

Keywords: crystallinity; growth mode; nano-confined region; OTFTs; pentacene

INTRODUCTION

The possibility of using organic semiconductors for electronic applications has been of great scientific and technological interest for several decades. The need for flexible electronics such as flexible displays, radio frequency identification tags and smart cards has been increasing because of the practical use of organic semiconductors in optoelectronic applications. The charge-carrier mobility of organic thin-film transistors (OTFTs) that use small molecules has improved considerably in response to optimization of deposition conditions, such as the deposition rate,^{1,2} substrate temperature,³ roughness⁴ and surface treatment.^{5,6} Organic electronic devices have also been reduced in size to the nano-scale and investigated for next-generation nano-electronic applications.^{7–11} Self-assembled nano-structures are of fundamental interest for understanding the structure-dependent properties of π -conjugated organic semiconductors.^{12,13} Molecular packing in the highly organized one-dimensional (1D) nano-structure of organic semiconductors is critical for determining charge transport mechanisms¹⁴ and the rational design of high-performance nano- and micro- electronic devices. However, to clarify the effects of active layer morphology on charge transport in organic semiconductor nano-devices, related

studies must be conducted at the nano-scale. Here, we investigated how the morphology of pentacene grown in nano- and micro-confined line patterns affects charge transport in OTFT, comparing with normal pentacene morphology with a terrace-like feature and an average grain size of $\sim 1.7\ \mu\text{m}$. To systematically investigate how the nano-confinement affects pentacene film growth and charge transport along electrodes, micro- and nano-confined photoresist (PR) patterns were fabricated by conventional photolithography and phase-shift soft lithography using a transparent poly(dimethylsiloxane) (PDMS) mold. Height of all the PR patterns were designed to be above 250 nm on the silicon dioxide (SiO₂) surfaces, instead of shallow nano-grooves,¹⁵ could minimize undesired contribution of pentacene crystals onto the PR patterns to the charge-carrier transport, providing the perfectly confined geometries to investigate the π -conjugated nanostructure of pentacene affecting the charge transport along the source–drain (*S–D*) electrode direction.

We then compared field-effect mobility (μ_{FET}) values of OTFTs containing pentacene crystals percolated in the confined patterns with those of the standard OTFTs. As the line spacing (L_S) between the tall PR reliefs decreased to below the average size of typical pentacene grains on smooth and organo-compatible dielectrics, μ_{FET} values of

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Received 5 July 2013; revised 27 November 2013; accepted 9 December 2013

top-contacted electrode OTFTs were considerably improved. Specifically, the μ_{FET} values for the 250 nm confined dielectric system were much higher ($0.33 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) than those of the micro-scale confined or flat dielectric systems ($\leq 0.15 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$). These improvements were related to enhancement of charge-carrier transport along the *S-D* electrodes oriented parallel to the PR lines, owing to the anisotropic intermolecular π -conjugation of pentacene nucleated from the nano-confined PR edges, providing important insight for the design of high-performance nano-scale organic electronics.

EXPERIMENTAL PROCEDURE

To demonstrate how the morphology of pentacene grown in confined regions affects charge transport, top-contact OTFTs were designed to contain nominally 50-nm-thick pentacene polycrystals confined onto poly(methyl methacrylate) (PMMA)-coated SiO_2 dielectrics between periodically patterned PR reliefs. First, PR films (AZ Electronic Materials USA Co., Somerville, NJ, USA) were spin-cast on heavily doped silicon wafers (Arsenic doped n-type Si) covered with thermally grown 100-nm-thick SiO_2 layers. Elastomeric PDMS masks were placed in direct contact with the PR films to form the micro- and nano-relief patterns by combining conventional photolithography with soft lithography (known as phase-shift lithography; see Supplementary Figure S1 in the Supporting Information). As the PDMS masks used in this study are transparent to ultraviolet light with a wavelength (λ) of $> 300 \text{ nm}$, the transmitted light identified by the refractive index of the PDMS (~ 1.43) is modulated with an in-phase mode, within the depth of the reliefs on the bottom side of the PDMS surface. In this case, minimum doses of the transmitted light appeared at the relief edges.^{16–18} Values of L_S , as the determining factor of the geometrical confinement, could be controlled to be 9 μm , 3 μm , 1 μm and 250 nm (see Figure 1 and Supplementary Figure S2). The patterned PR/ SiO_2 dielectrics were then treated with oxygen plasma (O_2 50 sccm, 30 mTorr) to eliminate the PR residues on the confined SiO_2 regions, and ultrathin PMMA ($M_w \sim 350\,000 \text{ g mol}^{-1}$) layers were spin-cast onto the dielectrics from 0.02 wt% toluene solution.

Pentacene (Polysis Pure Products Co., Seoul, Republic of Korea) was deposited on the substrates by an organic molecular-beam deposition system (with a quartz crystal balance to monitor nominal film thickness; under a base pressure of $\sim 10^{-6}$ Torr and substrate temperature of 30°C). Top-contacted Au electrodes were fabricated on the pentacene films, specific orientations of either parallel (*PL*) or perpendicular (*PP*) with respect to the PR reliefs (see Figure 2). Grazing-incidence X-ray diffraction (GIXD) was performed at the 10 C1 beamline ($\lambda = 1.54 \text{ \AA}$) of the Pohang Accelerator Laboratory, and atomic force microscopy (AFM) was conducted using a scanning probe microscope

(Multimode 8, Bruker, Santa Barbara, CA, USA) operated in tapping mode. The current–voltage (*I–V*) characteristics were measured under a nitrogen conditions using a Keithley 4200 semiconductor parameter analyzer (Keithley Instruments Inc., Cleveland, OH, USA).

RESULTS AND DISCUSSION

Self-assembly of organic semiconductors to form π -conjugated orientation preferential to the charge transport direction may be one of the best methods of achieving high-performance OTFTs.¹⁵ To determine the effects of confinement on the crystal growth of pentacene showing terrace-like grains (with an average size of 1.7 μm on the PMMA-coated SiO_2 dielectrics; see Figure 3a) and the electrical properties of the resulting crystals in OTFT, various confined geometries on the PMMA-coated SiO_2 dielectrics were manipulated by line-patterned PR reliefs $L_S = 250 \text{ nm}$, 1 μm , 3 μm and 9 μm , respectively (see Figure 1 and Supplementary Figure S2). Because the PR reliefs with a constant periodicity were much taller (250–450 nm) than the SiO_2 dielectric layer, the gate voltage (V_G)-induced electric field within PMMA-coated PR/ SiO_2 regions was much lower than that within the PMMA-coated SiO_2 dielectrics. As a result, the PR patterned geometries provided environmental conditions that enabled investigation of the charge transport behavior of OTFTs containing the pentacene crystals fabricated on the confined geometries (discussed below). However, rough PR surfaces were found to cause less-ordered pentacene aggregates with small grains (200–300 nm) even after the organo-compatible PMMA layers were introduced (see Figure 3b).

Here, two types of top-contacted Au electrodes were fabricated to be oriented with either *PL* or *PP* to the charge transport direction (see Figure 2). As values of L_S with the PMMA- SiO_2 surfaces decreased to below a critical value (expected to be $\sim 1.7 \mu\text{m}$), the growth mode of pentacene was found to be a three-dimensional (3D) island instead of Stranski–Krastanov mode (or layer-by-island). Interestingly, the highest value of μ_{FET} was indicated for OTFTs containing pentacene crystals percolated in nano-confined geometry (with $L_S = 250 \text{ nm}$) in comparison with other OTFTs. Below, we discuss how the confinement-driven crystal growth of pentacene affects the charge transport behavior along the *S–D* electrodes.

Micro-scale PR/ SiO_2 substrates fabricated using conventional photo-lithography contained periodically alternated PR and SiO_2 regions (with values of L_S ranging from 1 to 9 μm ; see Supplementary Figure S2). In contrast, periodic PR line patterns with a 2- μm pitch and $L_S = 250 \text{ nm}$ (see Figure 1b) could be manipulated on the SiO_2 dielectrics using phase-shift lithography as described in the Supporting Information (see Supplementary Figure S1). Because all PR line patterns possessed considerable heights, these confined patterns were expected to have significant effects on the π -conjugated self-assembly of pentacene along the long axis of the PR patterns oriented either *PL* or *PP* to the charge transport direction, that is, the *S–D* electrode direction. Pentacene films were developed with a layer-by-island growth mode on the PMMA-coated SiO_2 dielectrics, showing terrace-like crystals with an average grain size of $\sim 1.7 \mu\text{m}$, whereas on the PMMA-coated PR surfaces, 3D pentacene grains (200–300 nm) were observed (see Figure 3). In addition, the layer-by-island growth mode of pentacene tended to be changed to a 3D island growth at $L_S < \text{normal grain size}$ ($\sim 1.7 \mu\text{m}$; see Supplementary Figures S3 and S4).

The electrical performance of pentacene TFTs based on the micro- and nano-confined geometries was compared with that of control devices on both the PMMA-coated SiO_2 and PR- SiO_2 dielectrics. In addition, variations in charge transport depending on the *S–D*

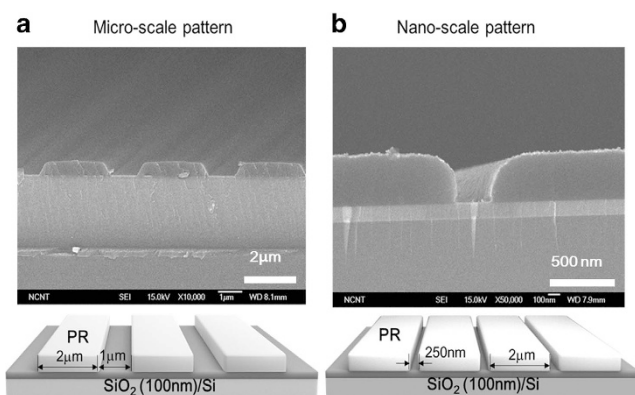


Figure 1 Scanning electron microscopy (SEM) images of photoresist (PR) pattern. (a) Micro-scale patterns consist of similarly spaced PR and silicon dioxide (SiO_2) surface-modified poly(methyl methacrylate) (PMMA) thin-film alternately. (b) Nano-scale patterns consist of 2 μm width PR and $\sim 250 \text{ nm}$ SiO_2 layer, alternately. The heights of micro- and nano-scale patterns are 450 nm and 250 nm, respectively.

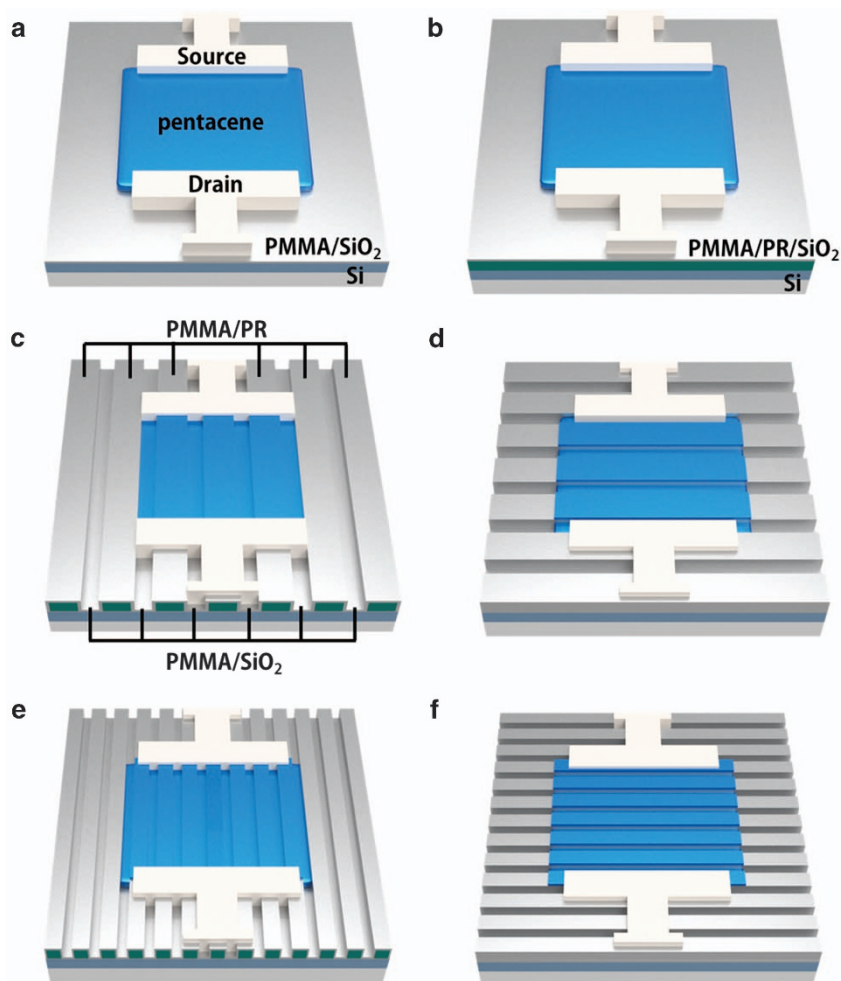


Figure 2 Schematic of the device configurations. Nonpatterned devices employed (a) the poly(methyl methacrylate) (PMMA)-coated silicon dioxide (SiO_2) or (b) PMMA-coated photoresist (PR) film as dielectrics. Patterned devices have (c, d) micro-spaced or (e, f) nano-spaced PR line patterns. (c, e) Parallel (PL) and (d, f) perpendicular (PP) stand for the directional relation between the charge transport and line pattern direction. The devices are classified according to the line pattern width and the direction between the charge transport and patterned line direction.

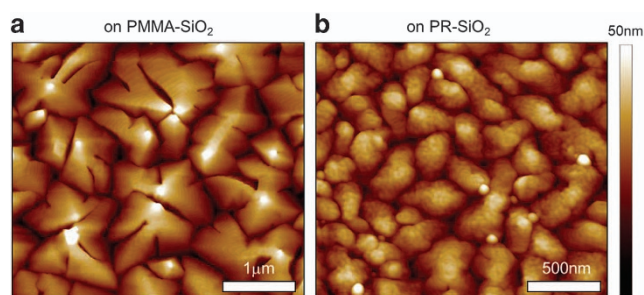


Figure 3 Atomic force microscopy (AFM) images of pentacene film (a) on the poly(methyl methacrylate) (PMMA)-coated silicon dioxide (SiO_2) surface and (b) PMMA-coated photoresist (PR) film surface. The average grain size of pentacene is $1.7 \mu\text{m}$ on the SiO_2 surface and $\sim 200 \text{ nm}$ on the PR film.

electrode direction, that is, PL and PP with respect to the PR patterns, were investigated (see Figure 4). It has been reported that shallow ($\sim 30 \text{ nm}$) periodic patterns induce preferred π -conjugation of pentacene along the S – D electrodes (parallel to the line patterns) during film growth in OTFT;¹⁵ in this case, the charge transport was drastically enhanced and showed much higher μ_{FET} values, relative to

the preferred π -conjugation perpendicular to the S – D electrode. The pentacene OTFTs on the PMMA-coated PR/ SiO_2 dielectrics with a high surface roughness (root-mean-square roughness, $R_q = 5.63 \text{ nm}$; channel length = $100 \mu\text{m}$; channel width = $1500 \mu\text{m}$) yielded poor μ_{FET} values of $0.017 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, resulting from the less-ordered π -conjugation of pentacene (see Figure 3b) that was also determined by GIXD (see Figure 5).

When the drain current (I_D)–gate voltage (V_G) transfer curves of the control devices based on the PMMA-coated SiO_2 and PR/ SiO_2 dielectrics were compared, the contribution of the pentacene grains percolated on the PMMA- SiO_2 sides to the total I_D (that is, charge transport) was almost two orders of magnitude higher than that on the PMMA-PR/ SiO_2 sides; for top-contact PL electrode OTFTs, the charge transport from the PR/ SiO_2 regions could be negligible. To calculate μ_{FET} in the micro- and nano-scale confined systems, the active conducting channel width (W), excluding the PR/ SiO_2 regions, was used as follows: for this calculation, the values of W for the PR-patterned SiO_2 dielectrics were $675 \mu\text{m}$ (for $L_S = 9 \mu\text{m}$), $502.5 \mu\text{m}$ (for $L_S = 3 \mu\text{m}$), $375 \mu\text{m}$ (for $L_S = 1 \mu\text{m}$) and $136 \mu\text{m}$ (for $L_S = 250 \text{ nm}$), respectively.

The I – V curves of the pentacene TFTs were measured in darkness at room temperature in a nitrogen atmosphere. I_D – V_G transfer

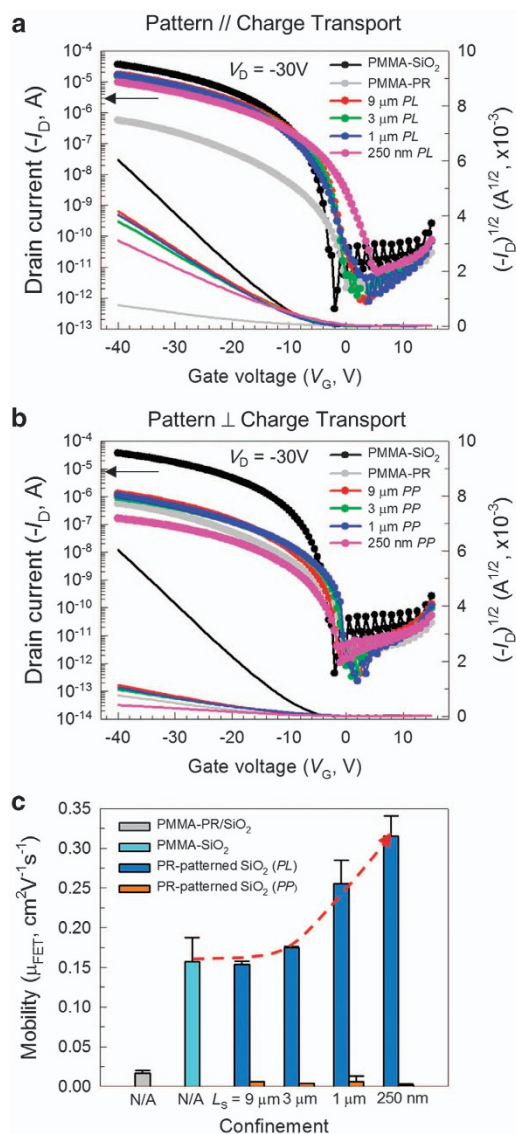


Figure 4 Electrical transfer characteristics (a, b) and field-effect mobility (c) of pentacene thin-film transistors (TFTs) within confined regions having different spaces. Devices with the direction of patterns (a) parallel and (b) perpendicular to the direction of charge transport in the channel. Gate voltage was swept at constant drain-source voltage of -30 V. The field-effect mobilities of 9 and $3 \mu\text{m}$ patterned devices were similar to those of the nonpatterned device (poly(methyl methacrylate) (PMMA)-coated silicon dioxide (SiO₂)) because the wider patterns have no effect of the confined region, but the field-effect mobilities of $1 \mu\text{m}$ and nanometer-scale patterned devices were higher than those of nonpatterned device.

characteristics (see Figures 4a and b) of the OTFTs were measured at a constant drain voltage (V_D) of -30 V (that is, in the saturation regime), and values of μ_{FET} were calculated in this regime.^{19–21} Other electrical parameters such as the on/off current ratio ($I_{\text{on}}/I_{\text{off}}$), threshold voltage (V_T) and sub-threshold swing (SS) were extracted from Figure 4 and summarized in Table 1. As L_S decreased down to $3 \mu\text{m}$, values of μ_{FET} for the top-contacted PL electrode OTFTs seemed to be steady. However, below $L_S = 3 \mu\text{m}$, they were suddenly increased. Particularly, μ_{FET} value of the nano-scale confined pentacene TFT ($L_S = 250$ nm), $0.333 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ was higher than that ($0.151 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$) of the control device on the PMMA-coated SiO₂ dielectric. This result suggests that the nano-confined geometry along

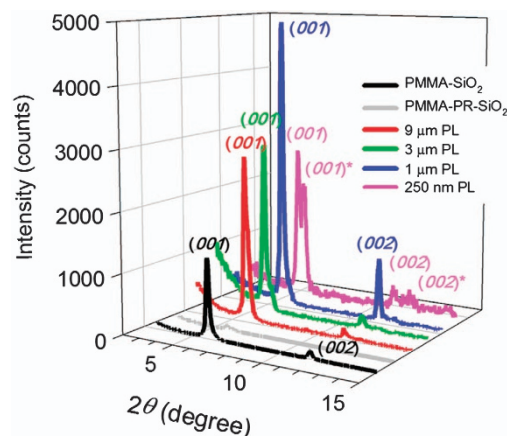


Figure 5 Grazing-incidence X-ray diffraction (GIXD) patterns for pentacene film with 50-nm thickness deposited on the poly(methyl methacrylate) (PMMA)-coated silicon dioxide (SiO₂), PMMA-coated photoresist (PR) film and PMMA-coated patterned PR/SiO₂ surfaces. We applied the geometric factor of the confined line spaces made by PR to calculate the data of GIXD.

the charge transport direction induces an anisotropic π -conjugated self-assembly of pentacene along the S – D electrodes. As shown in Figure 4c, the transition in μ_{FET} was indicated at $L_S = 1 \mu\text{m}$, and related to the crystal development of pentacene in the confined geometries; in this case, preferred crystal growing can be along the charge transport direction.

To interpret the relationship between the confinement-driven crystal structure and charge transport, AFM and GIXD analyses were systematically performed for various thick pentacene films on all of the dielectric surfaces. AFM topographies first indicated that pentacene films on PMMA-coated SiO₂ dielectrics grew in a manner that differed from that on PR/SiO₂ dielectrics (see Supplementary Figure S5). As shown in Supplementary Figure S5a, typical layer-by-island-grown pentacene crystals were observed on the PMMA-coated SiO₂ surfaces.²² In this case, pentacene molecules were more strongly bound to the substrate than to each other ($W_A > 2\gamma_p$, where W_A is the work of adhesion and γ_p is the surface energy of the pentacene crystal plane), and the seeding molecules are condensed to form the first molecular layer (ML) on the surface.²³ For layer growth (or island growth), $\gamma_i + \gamma_p < \gamma_g$ (or $\gamma_i + \gamma_p > \gamma_g$). Here, γ_i , γ_p and γ_g are the interfacial energy, surface energy of pentacene thin-film and gate dielectrics, respectively. If we introduce the term, work of adhesion W_A , then $W_A = \gamma_p + \gamma_g - \gamma_i$. By eliminating γ_i , $W_A > 2\gamma_p$ ($W_A < 2\gamma_p$) for layer-by-layer growth (or island growth). The $2\gamma_p$ is work of cohesion of pentacene. In contrast, on the rough PMMA-coated PR/SiO₂ dielectrics, 3D aggregates started to be grown at an initial stage without forming ML, that is, with a 3D island growth mode (see Supplementary Figure S5b), but they showed irregular grains with a nearly amorphous structure (determined by GIXD, see Figure 5), explaining the poor electrical performance ($0.017 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$). The surface heterogeneity of gate dielectrics also affects the crystal growth of organic semiconductors.^{24–30} On the 250-nm and $1 \mu\text{m}$ -confined PR-patterned SiO₂ dielectrics, pentacene started to be nucleated at the bottom-contacted edges of the PR reliefs as thermodynamically active nucleation sites.^{15,31} The pentacene grains were also reported to be elongated along the longer axis (less-confined direction) of the nano-confined geometry.¹⁵ The anisotropic grain morphology of pentacene could be observed for several nm-thick pentacene films on the 250-nm-confined system (see Supplementary Figures S3 and S4).

Table 1 Extracted other electrical parameters of pentacene FETs

Parameter	SiO ₂ film	PR film	9 μm PL	9 μm PP	3 μm PL	3 μm PP	1 μm PL	1 μm PP	nm PL	nm PP
I_{on}/I_{off}	8.3×10^7	2.7×10^5	1.8×10^7	9.7×10^5	3.0×10^8	2.8×10^6	4.1×10^7	8.5×10^6	1.5×10^6	1.5×10^5
SS	0.667	3.468	1.174	1.908	0.978	1.854	1.454	1.902	1.987	3.717
V_T	-6.620	-5.260	-4.137	-7.158	-3.242	-5.452	-5.088	-9.158	-4.770	-2.459
Mobility	0.151	0.020	0.158	0.006	0.176	0.004	0.279	0.006	0.333	0.001

Abbreviations: FETs, field-effect transistors; I_{on}/I_{off} , on/off current ratio; Mobility, field-effect mobility ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$); PL, parallel; PP, perpendicular; PR, photoresist; SiO₂, silicon dioxide; SS, sub-threshold swing (V dec^{-1}); V_T , threshold voltage (V).

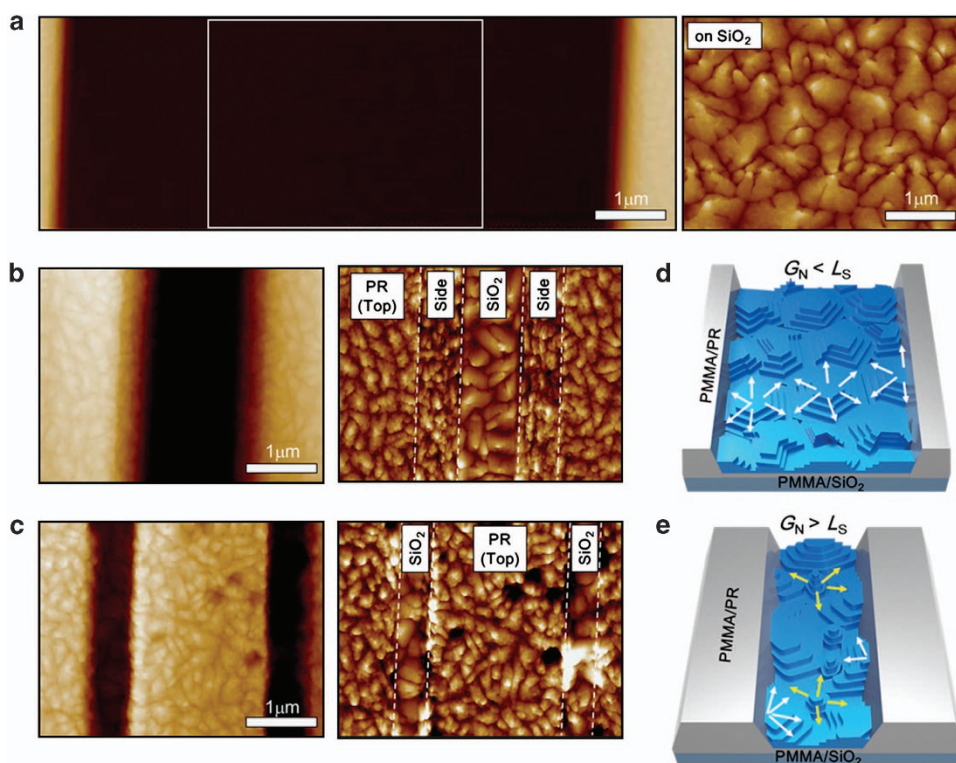


Figure 6 (a–c) Atomic force microscopy (AFM) topographies of 30-nm-thick pentacene thin films on the different photoresist (PR) patterned substrates: (a) $L_S = 9 \mu\text{m}$; (b) $L_S = 1 \mu\text{m}$; (c) $L_S = 250 \text{ nm}$, respectively. (d, e) Schematic illustration of pentacene growth in the confined region.

As mentioned in the Experimental Section, the successive procedures of PR patterning, O₂-plasma treatment and PMMA coating could form the patterned PR barriers with a height (micro-pattern: $\sim 450 \text{ nm}$; nano-pattern: $\sim 250 \text{ nm}$) sufficient to produce the perfectly confined SiO₂ dielectric surfaces with smooth and organo-compatible characteristics. It should be noted that some pentacene morphologies were not clearly detected using AFM with a polygonal-shaped probe tip because of the deep valley-like geometries; therefore, scanning electron microscopy was also used as a complementary tool (see Supplementary Figure S4). AFM analyses of the pentacene films on the PMMA-coated PR-patterned SiO₂ dielectrics revealed that the crystal growth mechanism of pentacene could be changed via controlling the degree of the geometrical confinement. When L_S is sufficiently wider than the normal grain size (G_N) of pentacene, crystal nucleation of pentacene occurs simultaneously at both the PR barrier edges and PMMA-coated SiO₂ surfaces (see Supplementary Figure S6) and then the crystals are growing laterally with a radial direction until they are percolated with the neighbors (see arrow-marked directions in Figures 6d and e). After the lateral crystal percolation, vertical crystal growth becomes dominant, showing

pentacene crystals with vertically terrace-like steps (see Figures 6a and d). In contrast, when $L_S < G_N$, most nuclei seem to appear at the PR barrier edges and the crystal growing prefers the less-confined open space perpendicular to the PR barriers, indicating elongated crystal grains along the growing direction (see Supplementary Figures S3 and S4). In OTFTs, charge-carrier transport is limited mainly within a several-nm-thick semiconducting layer that directly contacts the dielectric.^{32–35} As the pentacene film becomes thicker, vertically grown crystalline islands are percolated in comparison with the irregular aggregates on the top-most PR surfaces (see Figures 6b, c and e). As a result, suggesting that the unconventional crystal growth induces anisotropic π -overlap of pentacene along the percolated crystals in the nano-confined geometries.

In addition, 1D out-of-plane GIXD profiles were obtained for the 50-nm-thick pentacene films deposited on all of the dielectrics (see Figure 5). All out-of-plane X-ray peaks were indexed as (00l) and (00l)* crystal planes originating from the ‘thin film phase’ with a pseudo-orthorhombic unit cell and the ‘bulk phase’ with a triclinic unit cell, respectively. The inter-planar spacing of (001) was $d_{(001)} = 15.3 \text{ \AA}$ and $d_{(001)^*} = 14.2 \text{ \AA}$.^{36,37} It should be noted that

the lateral width of the incident X-ray beam used for GIXD ($<300\text{ }\mu\text{m}$) was much wider than all of the L_s , and the resulting GIXD profiles contained the crystal information on both the PMMA-coated PR/SiO₂ and SiO₂ regions. Fortunately, it was found that the pentacene aggregates on the topmost PR/SiO₂ surfaces had almost amorphous-like structure, as determined by GIXD analysis (gray solid lines in Figure 5).

Interestingly, the peak intensities of X-ray reflections from the micro- and nano-scale confined systems were much higher than those from the PMMA-coated SiO₂ system. Particularly, the 1D GIXD profile of the 250-nm-confined sample showed the X-ray reflections of both $(00l)$ and $(00l)^*$ crystal planes with abnormally high intensities owing to its lower volume fraction of the nano-confined regions of ~ 0.09 ($=136\text{ }\mu\text{m}/1500\text{ }\mu\text{m}$). The confinement effect decreased with an increase in L_s . There are two main factors affecting the X-ray reflections: scattering volume and crystallinity. The crystal growth of pentacene on the smooth PMMA-SiO₂ surface might be much faster than that on the uneven PMMA-PR surface. In this case, the actual thicknesses of the pentacene crystals grown in the confined area might be thicker than the nominal thicknesses monitored by the Quartz crystal balance during film deposition. However, the highly ordered X-ray reflections of the $1\text{-}\mu\text{m}$ patterned sample could not be explained only with the scattering volume effect, suggesting the following possibility; the asymmetrically micro- and nano-confined geometries can drive the self-assembly of pentacene molecules to form highly π -conjugated and crystalline structures, in comparison with flat or less-confined geometries, where there exist random nucleation sites and radial crystal growth of organic semiconductors.

For example, the dendritic- or pyramid-shaped crystals of pentacene on the PMMA-coated SiO₂ surface had many lateral grain boundaries (see Figure 6a), where the π -conjugation between the molecules is intrinsically mismatched. In contrast, pentacene started to grow initially at the PR edges, forming percolated crystal layer (related to $(00l)$ crystal reflection), and further grew into highly compact crystals (see yellow-marked directions in Figure 6e): in this case, the portion of the 'bulk phase' corresponding to $(00l)^*$ reflections tends to increase during filling the confined geometry (see Figures 6b and c).

Therefore, the morphological and X-ray results strongly support that inside the asymmetrically confined geometries, pentacene is crystallized from the patterned PR edges and its crystals contain π -conjugated planes preferentially oriented to the charge transport direction; the π - π stacking of pentacene molecules in the direction of charge transport increased as the patterned spaces became narrower. This type of confinement-induced molecular stacking of pentacene enhanced the charge transport in OTFT. As a result, the field-effect mobility of the device made of pentacene films grown in the 250-nm patterned region was approximately two times greater than those of the devices made from films grown in the unpatterned and micro ($9\text{-}3\text{ }\mu\text{m}$)-patterned region.

CONCLUDING REMARKS

We analyzed how the morphologies of organic semiconductor films confined in the micro- and nano-scale line and space relief patterns affect charge transport. As the patterned space region for confining the growth of organic semiconductors decreased below the average grain size ($\sim 1.7\text{ }\mu\text{m}$), the field-effect mobility increased by improving molecular ordering in the direction of charge transport because of increased confinement in the relief pattern. The field-effect mobility of the pentacene TFT in nano-confined regions (250 nm) was higher ($0.333\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$) than that of the normal thin-film device

($0.151\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$). We observed a transition of the field-effect mobility at $\sim 1\text{ }\mu\text{m}$ for the confined pattern, in which the patterned space is smaller than the normal grain size in thin films ($\sim 1.7\text{ }\mu\text{m}$). This transition indicates that molecular ordering is influenced by the pattern's confining effect on pentacene film growth. The results presented herein provide an approach that can be used to further increase the charge transport mobility of polycrystalline organic semiconductors by increasing the molecular ordering in the direction of charge transport. Furthermore, the organic semiconductor well confined in nano-structures is very similar to 1D nanowires because tall PR patterns prohibit charge transport perpendicular to the direction of S - D electrodes. The increased mobility of the transistors using pentacene grown in 1D nano-confined regions implies that 1D nanostructures of organic semiconductors can possess better molecular ordering and thus higher mobility than devices containing their thin-film counterparts.

ACKNOWLEDGEMENTS

This work was supported a grant (Code No. 2013M3A6A5073175) from the Center for Advanced Soft Electronics under the Global Frontier Research Program of the Ministry of Science, ICT and Future Planning, Korea. This research was also supported by the Pioneer Research Center Program through the National Research Foundation (NRF) of Korea funded by the Ministry of Science, ICT and Future Planning (2012-0009460) and supported by Basic Science Research Program through the National Research Foundation of Korea funded by the Ministry of Education (NRF-2013R1A1A2012660).

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